

GENERAL DESCRIPTION

CM6502S is a ZVS-Like Single PFC and it is designed to meet 90+ spec. (total efficiency). It has the following key features.

- 1.) Around 2% efficiency gain when the output load is below 40% of the full load.
- 2.) Hold Up time can be increased ~ 30% from the existing 6800 power supply.
- 3.) 420V bulk capacitor value can be reduced, and also PFC boost ripple current can be reduced; therefore, the boost inductor core size may be reduced.
- 4.) No Load Consumption can be reduced to 290mW at 270VAC.
- 5.) The stress over the entire external power device is reduced and EMI noise reduced.
- 6.) A PGB function is designed for interfacing to next stage controller. It has a customer programmable low threshold PGTHL.

CM6502S is designed to meet the EPA/80+ regulation. With the proper design, its efficiency of power supply can easily approach 90+.

FEATURES

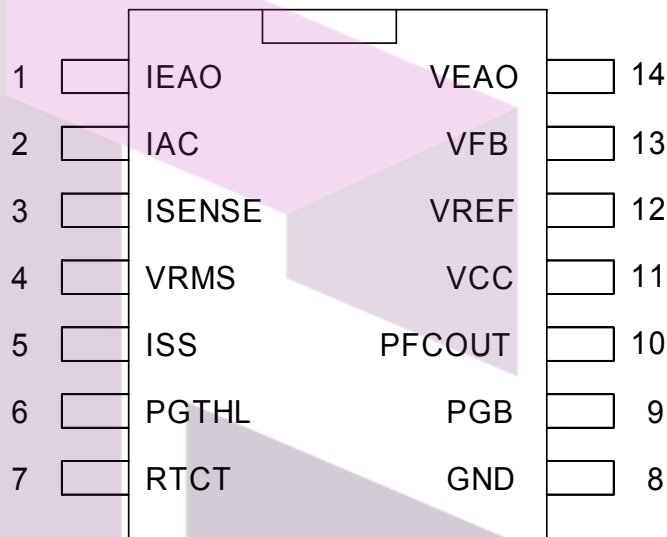
- ◆ Patents Pending
- ◆ 23V Bi-CMOS process.
- ◆ Designed for EPA/90+efficiency.
- ◆ Selectable Boost output from 380V to 342V during light load.
- ◆ All high voltage resistors can be greater than 5 Mega ohm (5 Mega to 8 Mega ohm) to improve the no load consumption.
- ◆ Rail to rail CMOS Drivers with on, 60 ohm and off, 30 ohm with 17V zeners.
- ◆ Fast Start-UP Circuit without extra bleed resistor to aid VCC reaches 13V sooner.
- ◆ Low start-up current (55uA typ.)
- ◆ Low operating current (2.5mA typ.)
- ◆ 16.5V VCC shunt regulator
- ◆ Dynamic Soft PFC to ease the stress of the Power Device and Ease the EMI-filter design.
- ◆ PFC Digital Brown Out
- ◆ Low total harmonic distortion, THD and Power Factor approaches 1.0.
- ◆ Average current, continuous or discontinuous boost leading edge PFC.
- ◆ Current fed Gain Modulator for improved noise immunity.
- ◆ Gain Modulator is a constant maximum power limiter.
- ◆ Brown-out control, over-voltage protection, UVLO, and soft start, and Reference OK.
- ◆ Power Fold Back Protection

APPLICATIONS

- ◆ EPA/90+ related Power Supply
- ◆ Desktop PC Power Supply
- ◆ Internet Server Power Supply
- ◆ LCD Power Supply
- ◆ PDP Power Supply
- ◆ IPC Power Supply
- ◆ UPS
- ◆ Battery Charger
- ◆ DC Motor Power Supply
- ◆ Monitor Power Supply
- ◆ Telecom System Power Supply
- ◆ Distributed Power

PIN CONFIGURATION

SOP-14 (S14)

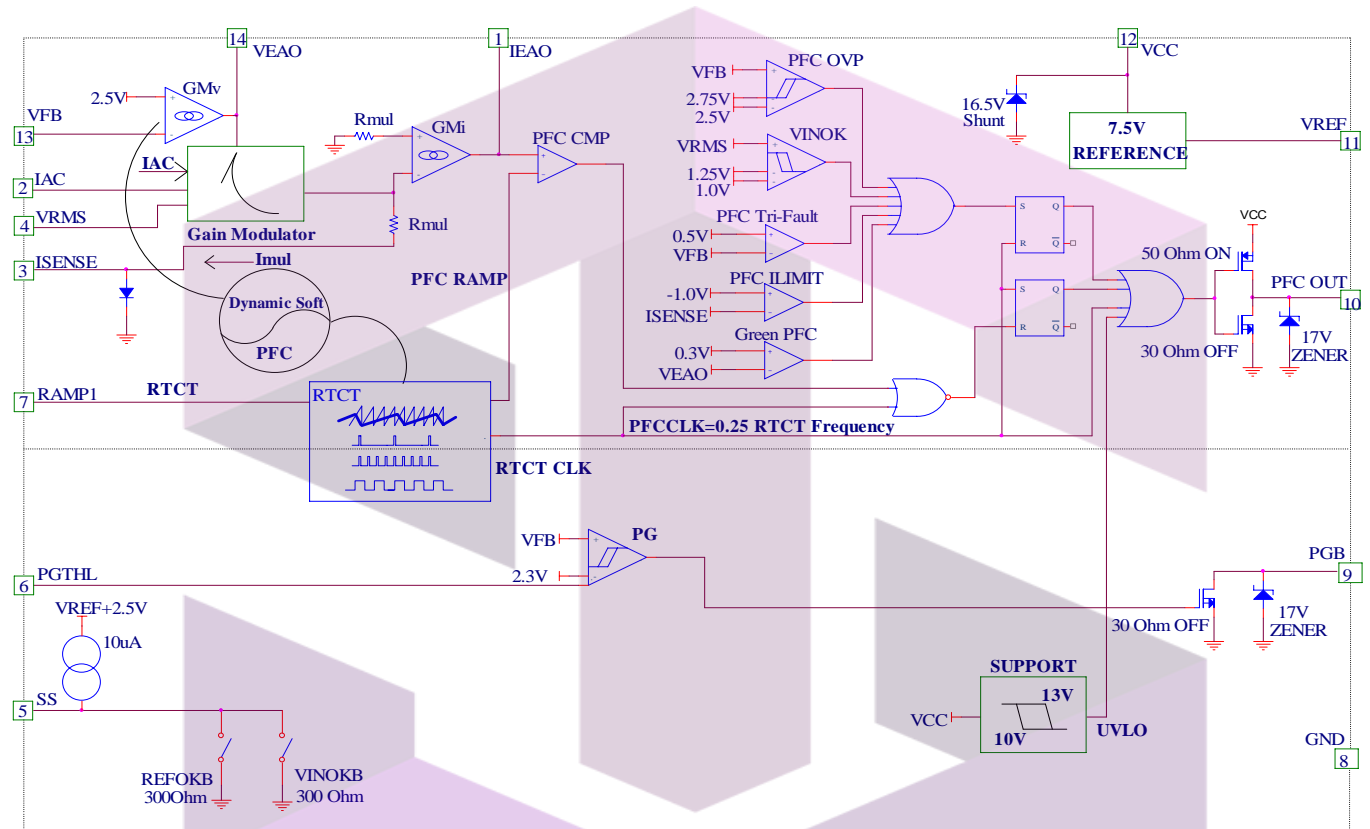


PIN DESCRIPTION

Pin No.	Symbol	Description	Operating Voltage			
			Min.	Typ.	Max.	Unit
1	IEAO	PFC transconductance current error amplifier output (Gmi).	0		VREF	V
2	IAC	IAC has 2 functions: 1. PFC gain modulator reference input. 2. At start up, IAC is connected to VCC and it helps to reduce the startup time and it helps to reduce the no load consumption. Typical RAC resistor is about 6 Mega ohm to 8 Mega ohm to sense the line.	0		100	uA
3	ISENSE	PFC Current Sense: for both Gain Modulator and PFC ILIMIT comparator.	-1.2		0.7	V
4	VRMS	Line Input Sense pin for multiplier and also it is the brown out sense pin.	0		6	V
5	ISS	PFC Soft Start pin: It supplies ~ 10uA to SS pin. It provides a close-loop soft start function during power supply start up. PFC Soft Start function can just need a simple capacitor to ground and it can be around 1uF	0		10	V

6	PGTHL	PGTHL is an input I/O. The user can program the Low Threshold of the Power Good which can determine the comparator output of PGB(open drain) to be pulled high.	0		2.3	V
7	RTCT	Oscillator timing node; timing set by RT and CT	0.8		4	V
8	GND	Ground				
9	PGB	PGB is the PG comparator output. The input of PG comparator is using Vfb (pin 13) to compare with the high threshold, 2.3V (preset internally) and the low threshold, PGTHL (pin 6, Set by user). When 380V is ready, pin 9 is open-drain and it will be pulled low.	0		6	V
10	PFC OUT	PFC driver output	0		VCC	V
11	V _{CC}	Positive supply for CM6502S	10	15	18	V
12	VREF	Maximum 3.5mA buffered output for the internal 7.5V reference when VCC=14V		7.5		V
13	V _{FB}	PFC transconductance voltage error amplifier input	0	2.5	3	V
14	VEAO	PFC transconductance voltage error amplifier output (GmV)	0		6	V

Simplified Block Diagram (CM6502S)



ORDERING INFORMATION

Part Number	Temperature Range	Package
CM6502SGIS*	-40°C to 125°C	14-Pin Narrow SOP (S14)

*Note: G : Suffix for Pb Free Product

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are those values beyond which the device could be permanently damaged.

Parameter	Min.	Max.	Units
V _{CC}		18	V
IEAO	0	VREF+0.3	V
ISENSE Voltage	-5	0.7	V
PFC OUT	GND - 0.3	VCC + 0.3	V
I _{REF}		5	mA
I _{AC} Input Current		1	mA
Peak PFC OUT Current, Source or Sink		0.5	A
PFC OUT, Energy Per Cycle		1.5	μJ
Junction Temperature		150	°C
Storage Temperature Range	-65	150	°C
Operating Temperature Range	-40	125	°C
Lead Temperature (Soldering, 10 sec)		260	°C
Thermal Resistance (θ _{JA})			
Plastic DIP		80	°C/W
Plastic SOIC		105	°C/W

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply $V_{CC}=+14V$, $R_T = 7.75K \text{ k}\Omega$, $C_T = 1000pF$, T_A =Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6502S			Unit
			Min.	Typ.	Max.	
PFC Brown Out						
	VRMS Threshold High	Room Temperature=25°C	1.19	1.25	1.32	V
	VRMS Threshold Low	Room Temperature=25°C	0.97	1.05	1.13	V
	Hysteresis		170	216	260	mV
	AC High Light	Sweep Vrms Pin	2.13	2.25	2.36	V
	AC Low Light	Sweep Vrms Pin	1.66		1.82	V
	Hysteresis		0.68		0.86	V
Voltage Error Amplifier (g _{mv})						
	Input Voltage Range		0		3	V
	Transconductance	V _{NONINV} = V _{INV} , VEO = 3.75V @ T=25°C	38	48	58	μ mho
	Feedback Reference Voltage (High)	Veao = 1.5V VRMS>2.25V	2.32	2.39	2.44	V
	Input Bias Current	Note 2	-1.0	-0.05		μ A
	Output High Voltage		5.8	6.0		V
	Output Low Voltage			0.1	0.4	V
	Sink Current	V _{FB} = 3V, VEO = 6V		6.7		μ A
	Source Current	V _{FB} = 1.5V, VEO = 1.5V	TBD	70	TBD	μ A
	Open Loop Gain	DC gain	30	40		dB
	Power Supply Rejection Ratio	11V < V _{CC} < 16.5V	60	75		dB
Current Error Amplifier (g _{mi})						
	Input Voltage Range (Isense pin)		-1.2		0.7	V
	Transconductance	V _{NONINV} = V _{INV} , IEAO = 3.75V @ T=25°C	50	65	80	μ mho
	Input Offset Voltage	VEAO=0V, IAC is open	-10		50	mV
	Output High Voltage		6.8	7.4	7.7	V
	Output Low Voltage			0.1	0.4	V

ELECTRICAL CHARACTERISTICS :

(Conti.) Unless otherwise stated, these specifications apply $V_{CC}=+14V$, $R_T = 7.75\text{ k}\Omega$, $C_T = 1000\text{pF}$, $T_A=\text{Operating Temperature Range (Note 1)}$

Symbol	Parameter	Test Conditions	CM6502S			Unit
			Min.	Typ.	Max.	
	Sink Current	$I_{SENSE} = +0.5V$, $IEAO = 4.0V$		-47	-20	μA
	Source Current	$I_{SENSE} = -0.5V$, $IEAO = 1.5V$	20	47		μA
	Open Loop Gain	DC Gain	30	40		dB
	Power Supply Rejection Ratio	$11V < V_{CC} < 16.5V$	60	75		dB
PFC OVP Comparator						
	Threshold Voltage		2.59	2.79	2.99	V
	Hysteresis		0.24	0.27	0.30	mV
PFC Green Power Detect Comparator						
	Veao Threshold Voltage		0.15	0.25	0.35	V
Tri-Fault Detect						
	Fault Detect HIGH		2.59	2.79	2.99	V
	Time to Fault Detect HIGH	$V_{FB}=V_{\text{FAULT DETECT LOW to}}$ $V_{FB}=\text{OPEN}$, 470pF from V_{FB} to GND		2	4	ms
	Fault Detect LOW		0.4		0.65	V
PFC I_{LIMIT} Comparator						
	Threshold Voltage		-1.10	-1.00	-0.90	V
	($PFC I_{\text{LIMIT}}$ — Gain Modulator Output)		100	200		mV
	Delay to Output (Note 4)	Overdrive Voltage = -100mV		700		ns

ELECTRICAL CHARACTERISTICS:

(Conti.) Unless otherwise stated, these specifications apply $V_{CC}=+14V$, $R_T = 7.75\text{ k}\Omega$, $C_T = 1000\text{pF}$, $T_A=\text{Operating Temperature Range (Note 1)}$

Symbol	Parameter	Test Conditions	CM6502S			Unit
			Min.	Typ.	Max.	
GAIN Modulator						
	Gain1 (Note 3)	$I_{AC} = 20\text{ }\mu\text{A}$, $V_{RMS} = 1.125$, $V_{FB} = 2.375V$ @ $T=25^{\circ}\text{C}$ SS<VREF	4.2	5.33	6.36	
	Gain2 (Note 3)	$I_{AC} = 20\text{ }\mu\text{A}$, $V_{RMS} = 1.45588V$, $V_{FB} = 2.375V$ @ $T=25^{\circ}\text{C}$ SS<VREF	3.36	4.15	5.04	
	Gain3 (Note 3)	$I_{AC} = 20\text{ }\mu\text{A}$, $V_{RMS} = 2.91V$, $V_{FB} = 2.375V$ @ $T=25^{\circ}\text{C}$ SS<VREF	1.3		1.8	
	Gain4 (Note 3)	$I_{AC} = 20\text{ }\mu\text{A}$, $V_{RMS} = 3.44V$, $V_{FB} = 2.375V$ @ $T=25^{\circ}\text{C}$ SS<VREF	1.0		1.45	
	Bandwidth (Note 4)	$I_{AC} = 40\text{ }\mu\text{A}$		1		MHz
	Output Voltage = $R_{mul} * (I_{SENSE}-I_{OFFSET})$	$I_{AC} = 50\text{ }\mu\text{A}$, $V_{RMS} = 1.125V$, $V_{FB} = 2.375V$ SS<VREF	0.7	0.78	0.87	V
Oscillator (Measuring fpfc)						
	Initial fpfc Accuracy 1	$R_T = 7.75\text{ k}\Omega$, $C_T = 1000pF$, $T_A = 25^{\circ}\text{C}$ $I_{AC}=0\mu A$	51	54.5	60	kHz
	Voltage Stability	$11V < V_{CC} < 16.5V$		2		%
	Temperature Stability			2		%
	Total Variation	Line, Temp	48		60	kHz
	Ramp Valley to Peak Voltage	$V_{EAO}=6V$ and $I_{AC}=20\mu A$		2.5		V
	PFC Dead Time (Note 4)		500		900	ns
	CT Discharge Current	$V_{RAMP2} = 0V$, $V_{RAMP1} = 2.5V$		10.5	15	mA
Light Load Veao Threshold						
	Light Load Threshold (High)	Room Temperature= 25°C	2.13	2.25	2.36	V
	Light Load Threshold (Low)	Room Temperature= 25°C	1.58	1.75	1.92	V
	Hysteresis		470	500	530	mV

ELECTRICAL CHARACTERISTICS (Conti.) Unless otherwise stated, these specifications apply
 $V_{CC}=+14V$, $R_T = 7.75k\Omega$, $C_T = 1000pF$, T_A =Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6502S			Unit
			Min.	Typ.	Max.	
Reference						
	Output Voltage	T _A = 25°C, I(VREF) = 0mA	7.3	7.5	7.7	V
	Line Regulation	11V < V _{CC} < 16.5V@ T=25°C		10	25	mV
	Load Regulation	VCC=10.5V,0mA < I(VREF) < 2.5mA; @ T=25°C		30	50	mV
		VCC=14V,0mA < I(VREF) < 3.5mA; T _A = -40°C~85°C		30	50	mV
	Temperature Stability			0.4		%
	Total Variation	Line, Load, Temp	7.2		7.8	V
	Long Term Stability	T _J = 125°C, 1000HRs	5		25	mV
PFC						
	Minimum Duty Cycle	IEAO > 4.5V			0	%
	Maximum Duty Cycle	V _{IEAO} < 1.2V	92	96.9		%
	Output Low Rdson	I _{OUT} = -20mA @ T=25°C		12	15	ohm
		I _{OUT} = -100mA @ T=25°C			15	ohm
		I _{OUT} = 10mA, V _{CC} = 9V @ T=25°C		0.5	1	V
	Output High Rdson	I _{OUT} = 20mA @ T=25°C		26.5	40	ohm
		I _{OUT} = 100mA @ T=25°C			40	ohm
	Rise/Fall Time (Note 4)	C _L = 100pF @ T=25°C		50		ns
Soft Start						
	Soft Start Current	Room Temperature=25°C	6	10	14	μA
Supply						
	Start-Up Current	V _{CC} = 12V, C _L = 0 @ T=25°C		55	80	μA
	Operating Current	14V, C _L = 0		2.6	5.0	mA
	Undervoltage Lockout Threshold	CM6502S	12.35	12.85	13.65	V
	Undervoltage Lockout Hysteresis	CM6502S	2.73	2.90	3.15	V
Shunt Regulator (VCC zener)						
	Zener Threshold Voltage	Apply VCC with Iop=20mA	16.2	16.75	17.4	V

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Includes all bias currents to other circuits connected to the V_{FB} pin.

Note 3: Gain $\sim K \times 5.3V$; $K = (I_{SENSE} - I_{OFFSET}) \times [I_{AC} (VEAO - 0.7)]^{-1}$; $VEAO_{MAX} = 6V$

Note 4: Guaranteed by design, not 100% production test.

Getting Start:

To start evaluating CM6502S from the exiting CM6800 or ML4800 board, 6 things need to be taken care before doing the fine tune:

- 1.) Change RAC resistor (on pin 2, IAC) from the old value to a higher resistor value between 6 Mega ohms to 8 Mega ohms.
- 2.) Change RTCT pin (pin 7) from the existing value to $RT=7.750K$ ohm and $CT=1000pF$ to have $f_{pfc}=55$ Khz, $f_{RTCT}=220Khz$ for CM6502S.
- 3.) Adjust all high voltage resistor around 5 mega ohm or higher.
- 4.) VRMS pin (pin 4) needs to be 1.125V at $V_{IN}=85VAC$ for universal input application from line input from 85VAC to 270VAC. Both poles for the Vrms of the CM6502S needs to substantially slow than CM6800 about 5 to 10 times.
- 5.) At full load, the average Veao needs to around 4.5V and the ripple on the Veao needs to be less than 250mV.
- 6.) Soft Start pin (pin 5), the soft start current has been reduced from CM6800's 20uA to CM6502S's 10uA. Soft Start capacitor can be reduced to 1/2 from your original CM6800 capacitor.

Functional Description

CM6502S is designed for high efficient power supply for both full load and light load. It is a ZVS-Like PFC supply controller.

The CM6502S is an average current controlled, continuous/discontinuous boost Power Factor Correction (PFC) which uses leading edge modulation.

In addition to power factor correction, a number of protection features have been built into the CM6502S. These include soft-start, PFC over-voltage protection, peak current limiting, brownout protection, duty cycle limiting, and under-voltage lockout.

Power Factor Correction

Power factor correction makes a nonlinear load look like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with and proportional to the line voltage, so the power factor is unity (one). A common class of nonlinear load is the input of most power supplies, which use a bridge rectifier and capacitive input filter fed from the line. The peak-charging effect, which occurs on the input filter capacitor in these supplies, causes brief high-amplitude pulses of current to flow from the power line, rather than a sinusoidal current in phase with the line voltage. Such supplies present a power factor to the line of less than one (i.e. they cause significant current harmonics of the power line frequency to appear at their input). If the input current drawn by such a supply (or any other nonlinear load) can be made to follow the input voltage in instantaneous amplitude, it will appear resistive to the AC line and a unity power factor will be achieved.

To hold the input current draw of a device drawing power from the AC line in phase with and proportional to the input voltage, a way must be found to prevent that device from loading the line except in proportion to the instantaneous line voltage. The PFC section of the CM6502S uses a boost-mode DC-DC converter to accomplish this. The input to the converter is the full wave rectified AC line voltage. No bulk filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges (at twice line frequency) from zero volts to the peak value of the AC input and back to zero. By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current drawn from the power line is proportional to the input line voltage. One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. A commonly used value is 385VDC, to allow for a high line of $270VAC_{rms}$. The other condition is that the current drawn from the line at any given instant must be proportional to the line voltage. Establishing a suitable voltage control loop for the converter, which in turn drives a current error amplifier and switching output driver satisfies the first of these requirements. The second requirement is met by using the rectified AC line voltage to modulate the output of the voltage control loop. Such modulation causes the current error amplifier to command a power stage current that varies directly with the input voltage. In order to prevent ripple, which will necessarily appear at the output of boost circuit (typically about 10VAC on a 385V DC level); from introducing distortion back through the voltage error amplifier, the bandwidth of the voltage loop is deliberately kept low. A final refinement is to adjust the overall gain of the PFC such to be proportional to $1/(V_{in} \times V_{in})$, which linearizes the transfer function of the system as the AC input to voltage varies.

Since the boost converter topology in the CM6502S PFC is of the current-averaging type, no slope compensation is required.

More exactly, the output current of the gain modulator is given by:

Dynamic Soft PFC (patent pending)

Besides all the goodies from CM6800A, Dynamic Soft PFC is the main feature of CM6502S. Dynamic Soft PFC is to improve the efficiency, to reduce power device stress, to ease EMI, and to ease the monotonic output design while it has the more protection such as the short circuit with power-foldback protection. Its unique sequential control maximizes the performance and the protections among steady state, transient and the power on/off conditions.

PFC Section:
Gain Modulator

Figure 1 shows a block diagram of the PFC section of the CM6502S. The gain modulator is the heart of the PFC, as it is this circuit block which controls the response of the current loop to line voltage waveform and frequency, rms line voltage, and PFC output voltages. There are three inputs to the gain modulator. These are:

1. A current representing the instantaneous input voltage (amplitude and wave-shape) to the PFC. The rectified AC input sine wave is converted to a proportional current via a resistor and is then fed into the gain modulator at I_{AC} . Sampling current in this way minimizes ground noise, as is required in high power switching power conversion environments. The gain modulator responds linearly to this current.
2. A voltage proportional to the long-term RMS AC line voltage, derived from the rectified line voltage after scaling and filtering. This signal is presented to the gain modulator at V_{RMS} . The gain modulator's output is inversely proportional to V_{RMS}^2 (except at unusually low values of V_{RMS} where special gain contouring takes over, to limit power dissipation of the circuit components under heavy brownout conditions). The relationship between V_{RMS} and gain is called K, and is illustrated in the Typical Performance Characteristics.
3. The output of the voltage error amplifier, VEAO. The gain modulator responds linearly to variations in this voltage.

The output of the gain modulator is a current signal, in the form of a full wave rectified sinusoid at twice the line frequency. This current is applied to the virtual-ground (negative) input of the current error amplifier. In this way the gain modulator forms the reference for the current error loop, and ultimately controls the instantaneous current draw of the PFC from the power line. The general formula of the output of the gain modulator is:

$$I_{mul} = \frac{I_{AC} \times (VEAO - 0.7V)}{V_{RMS}^2} \times \text{constant} \quad (1)$$

$$\text{Gain} = I_{mul} / I_{AC}$$

$$K = \text{Gain} / (VEAO - 0.7V)$$

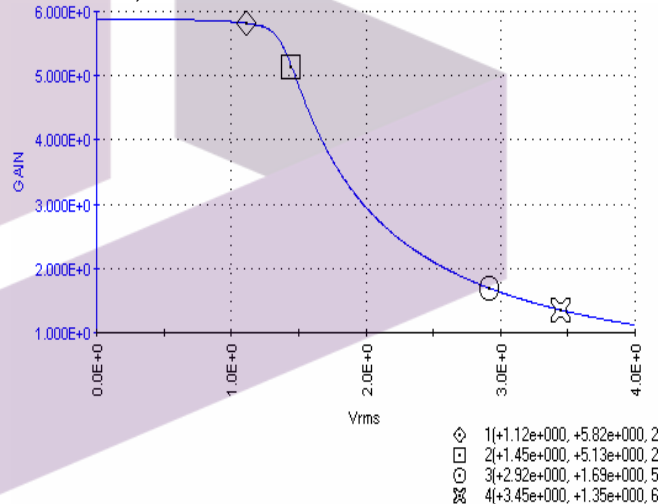
$$I_{mul} = K \times (VEAO - 0.7V) \times I_{AC}$$

Where K is in units of $[V^{-1}]$

Note that the output current of the gain modulator is limited around $140 \mu A$ and the maximum output voltage of the gain modulator is limited to $140 \mu A \times 5.7K = 0.8V$. This 0.8V also will determine the maximum input power.

However, $I_{GAINMOD}$ cannot be measured directly from I_{SENSE} . $I_{SENSE} = I_{GAINMOD} - I_{OFFSET}$ and I_{OFFSET} can only be measured when VEAO is less than 0.5V and $I_{GAINMOD}$ is 0A. Typical I_{OFFSET} is around 33uA.

$I_{AC} = 20 \mu A$, $Veao = 6V$



Gain vs. VRMS (pin4)

When V_{RMS} below 1V, the PFC is shut off. Designer needs to design 85VAC with V_{RMS} average voltage = 1.1225V.

$$\text{Gain} = \frac{I_{SENSE} - I_{OFFSET}}{I_{AC}} = \frac{I_{MUL}}{I_{AC}}$$

Selecting R_{AC} for I_{AC} pin

I_{AC} pin is the input of the gain modulator. I_{AC} also is a current mirror input and it requires current input. By selecting a proper resistor R_{AC} , it will provide a good sine wave current derived from the line voltage and it also helps program the maximum input power and minimum input line voltage.

$R_{AC} = V_{in \text{ min peak}} \times 50K$. For example, if the minimum line voltage is 85VAC, the $R_{AC} = 85 \times 1.414 \times 50K = 6 \text{ Mega ohm}$.

Vrms Description:

VRMS pin is designed for the following functions:

1. VRMS is used to detect the AC Brown Out (Also, we can call it PFC brown out.). When VRMS is less than 1.0 V +/-5%, PFCOUT will be turned off and VEA0 will be softly discharged toward 0 Volt. When VRMS is greater than 1.25V +/-5%, PFCOUT is enable and VEA0 is released.
2. VRMS also is used to determine if the AC Line is high line or it is low line. If VRMS is above 2.25V +/- 5%, IC will recognize it is high line the. If VRMS is below 2.0V +/- 5%, it is low line. Between $2.0V \leq V_{rms} \leq 2.25V$, it is the hysteresis.
3. At High Line and Light Load, 380V to 342V (Vfb threshold moves from 2.5V to 2.25V) is prohibited. At Low Line and Light Load, 380V to 342V (Vfb threshold moves from 2.5V to 2.25V) is enable. It provides ZVS-Like performance.
4. It is designed to provide the best THD and PF at high line since the gain is fixed. However, between -2.0V and 2.25V hysteresis region, it could be either way. Usually, it represents the line voltage between $V_{in} = 151V_{ac}$ and $V_{in} = 170V_{ac}$.

Current Error Amplifier, IEAO

The current error amplifier's output controls the PFC duty cycle to keep the average current through the boost inductor a linear function of the line voltage. At the inverting input to the current error amplifier, the output current of the gain modulator is summed with a current which results from a negative voltage being impressed upon the I_{SENSE} pin. The negative voltage on I_{SENSE} represents the sum of all currents flowing in the PFC circuit, and is typically derived from a current sense resistor in series with the negative terminal of the input bridge rectifier.

In higher power applications, two current transformers are sometimes used, one to monitor the IF of the boost diode. As stated above, the inverting input of the current error amplifier is a virtual ground. Given this fact, and the arrangement of the duty cycle modulator polarities internal to the PFC, an increase in positive current from the gain modulator will cause the output stage to increase its duty cycle until the voltage on I_{SENSE} is adequately negative to cancel this increased current. Similarly, if the gain modulator's output decreases, the output duty cycle will decrease, to achieve a less negative voltage on the I_{SENSE} pin.

PFC Brown Out (PFC Brown Out Comparator)

The PFC Brown Out comparator monitors the Vrms (pin 4) voltage and inhibits the PFC and PFC error amplifier output, Vea0 is pulled down during the Vrms is lower than threshold. If this voltage on Vrms is less than its nominal 1.25V. Once this voltage reaches 1.25V, which corresponds to the PFC input rms is around 88Vac. It is a hysteresis comparator and its lower threshold is 1V. After PFC Brown Out conditions are removed, the system will initiate the start up sequence with the proper soft start rate set by SS (pin 5).

Cycle-By-Cycle Current Limiter and Selecting R_{SENSE}

The I_{SENSE} pin, as well as being a part of the current feedback loop, is a direct input to the cycle-by-cycle current limiter for the PFC section. Should the input voltage at this pin ever be more negative than -1V, the output of the PFC will be disabled until the protection flip-flop is reset by the clock pulse at the start of the next PFC power cycle.

R_S is the sensing resistor of the PFC boost converter. During the steady state, line input current $\times R_{SENSE} = I_{mul} \times 5.7K$. Since the maximum output voltage of the gain modulator is $I_{mul} \max \times 5.7K = 0.8V$ during the steady state, $R_{SENSE} \times$ line input current will be limited below 0.8V as well. When VEA0 reaches maximum VEA0 which is 6V, I_{sense} can reach 0.8V. At 100% load, VEA0 should be around 4.5V and I_{SENSE} average peak is 0.6V. It will provide the optimal dynamic response + tolerance of the components.

Therefore, to choose R_{SENSE} , we use the following equation:

$$R_{SENSE} + R_{Parasitic} = 0.6V \times V_{inpeak} / (2 \times \text{Line Input power})$$

For example, if the minimum input voltage is 80VAC, and the maximum input rms power is 200Watt, $R_{SENSE} + R_{Parasitic} = (0.6V \times 80V \times 1.414) / (2 \times 200) = 0.169 \text{ ohm}$. The designer needs to consider the parasitic resistance and the margin of the power supply and dynamic response. Assume $R_{Parasitic} = 30 \text{ mOhm}$, $R_{SENSE} = 139 \text{ mOhm}$.

PFC OVP

In the CM6502S, PFC OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load should suddenly change. A resistor divider from the high voltage DC output of the PFC is fed to VFB. When the voltage on VFB exceeds 2.79V, the PFC output driver is shut down. The PWM section will continue to operate. The OVP comparator has 250mV of hysteresis, and the PFC will not restart until the voltage at VFB drops below 2.54V. The VFB power components and the CM6502S are within their safe operating voltages, but not so low as to interfere with the boost voltage regulation loop.

Error Amplifier Compensation

The PWM loading of the PFC can be modeled as a negative resistor; an increase in input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers. Figure 2 shows the types of compensation networks most commonly used for the voltage and current error amplifiers, along with their respective return points. The current loop compensation is returned to V_{REF} to produce a soft-start characteristic on the PFC: as the reference voltage comes up from zero volts, it creates a differentiated voltage on I_{EAO} which prevents the PFC from immediately demanding a full duty cycle on its boost converter.

PFC Voltage Loop

There are two major concerns when compensating the voltage loop error amplifier, V_{EAO} ; stability and transient response. Optimizing interaction between transient response and stability requires that the error amplifier's open-loop crossover frequency should be 1/2 that of the line frequency, or 23Hz for a 47Hz line (lowest anticipated international power frequency).

deviate from its 2.5V (nominal) value. If this happens, the transconductance of the voltage error amplifier, GM_V will increase significantly, as shown in the Typical Performance Characteristics. This raises the gain-bandwidth product of the voltage loop, resulting in a much more rapid voltage loop response to such perturbations than would occur with a conventional linear gain characteristics.

The Voltage Loop Gain (S)

$$= \frac{\Delta V_{OUT}}{\Delta V_{EAO}} * \frac{\Delta V_{FB}}{\Delta V_{OUT}} * \frac{\Delta V_{EAO}}{\Delta V_{FB}}$$

$$\approx \frac{P_{IN} * 2.5V}{V_{OUTDC}^2 * \Delta V_{EAO} * S * C_{DC}} * GM_V * Z_{CV}$$

Z_{CV} : Compensation Net Work for the Voltage Loop

GM_V : Transconductance of V_{EAO}

P_{IN} : Average PFC Input Power

V_{OUTDC} : PFC Boost Output Voltage; typical designed value is 380V.

C_{DC} : PFC Boost Output Capacitor

PFC Current Loop

The current transconductance amplifier, GM_I , I_{EAO} compensation is similar to that of the voltage error amplifier, V_{EAO} with exception of the choice of crossover frequency. The crossover frequency of the

current amplifier should be at least 10 times that of the voltage amplifier, to prevent interaction with the voltage loop. It should also be limited to less than 1/6th that of the switching frequency, e.g. 8.33kHz for a 50kHz switching frequency.

The Current Loop Gain (S)

$$= \frac{\Delta V_{ISENSE}}{\Delta D_{OFF}} * \frac{\Delta D_{OFF}}{\Delta I_{EAO}} * \frac{\Delta I_{EAO}}{\Delta I_{SENSE}}$$

$$\approx \frac{V_{OUTDC} * R_S}{S * L * 2.5V} * GM_I * Z_{CI}$$

Z_{CI} : Compensation Net Work for the Current Loop

GM_I : Transconductance of I_{EAO}

V_{OUTDC} : PFC Boost Output Voltage; typical designed value is 380V and we use the worst condition to calculate the Z_{CI}

R_{SENSE} : The Sensing Resistor of the Boost Converter

2.5V: The Amplitude of the PFC Leading Edge Modulation Ramp(typical)

L: The Boost Inductor

The gain vs. input voltage of the CM6502S's voltage error amplifier, V_{EAO} has a specially shaped non-linearity such that under steady-state operating conditions the transconductance of the error amplifier, GM_V is at a local minimum. Rapid perturbation in line or load conditions will cause the input to the voltage error amplifier (V_{FB}) to

I_{SENSE} Filter, the RC filter between R_{SENSE} and I_{SENSE} :

There are 2 purposes to add a filter at I_{SENSE} pin:

- 1.) Protection: During start up or inrush current conditions, it will have a large voltage cross R_S which is the sensing resistor of the PFC boost converter. It requires the I_{SENSE} Filter to attenuate the energy.
- 2.) To reduce L, the Boost Inductor: The I_{SENSE} Filter To reduce L, the Boost Inductor: The I_{SENSE} Filter also can reduce the Boost Inductor value since the I_{SENSE} Filter behaves like an integrator before going I_{SENSE} which is the input of the current error amplifier, I_{EAO} .

The I_{SENSE} Filter is a RC filter. The resistor value of the I_{SENSE} Filter is between 100 ohm and 50 ohm because $I_{OFFSET} \times$ the resistor can generate an offset voltage of I_{EAO} . By selecting R_{FILTER} equal to 50 ohm will keep the offset of the I_{EAO} less than 5mV. Usually, we design the pole of I_{SENSE} Filter at $f_{pfc}/6=8.33KHz$, one sixth of the PFC switching frequency. Therefore, the boost inductor can be reduced 6 times without disturbing the stability. Therefore, the capacitor of the I_{SENSE} Filter, C_{FILTER} , will be around 381nF.

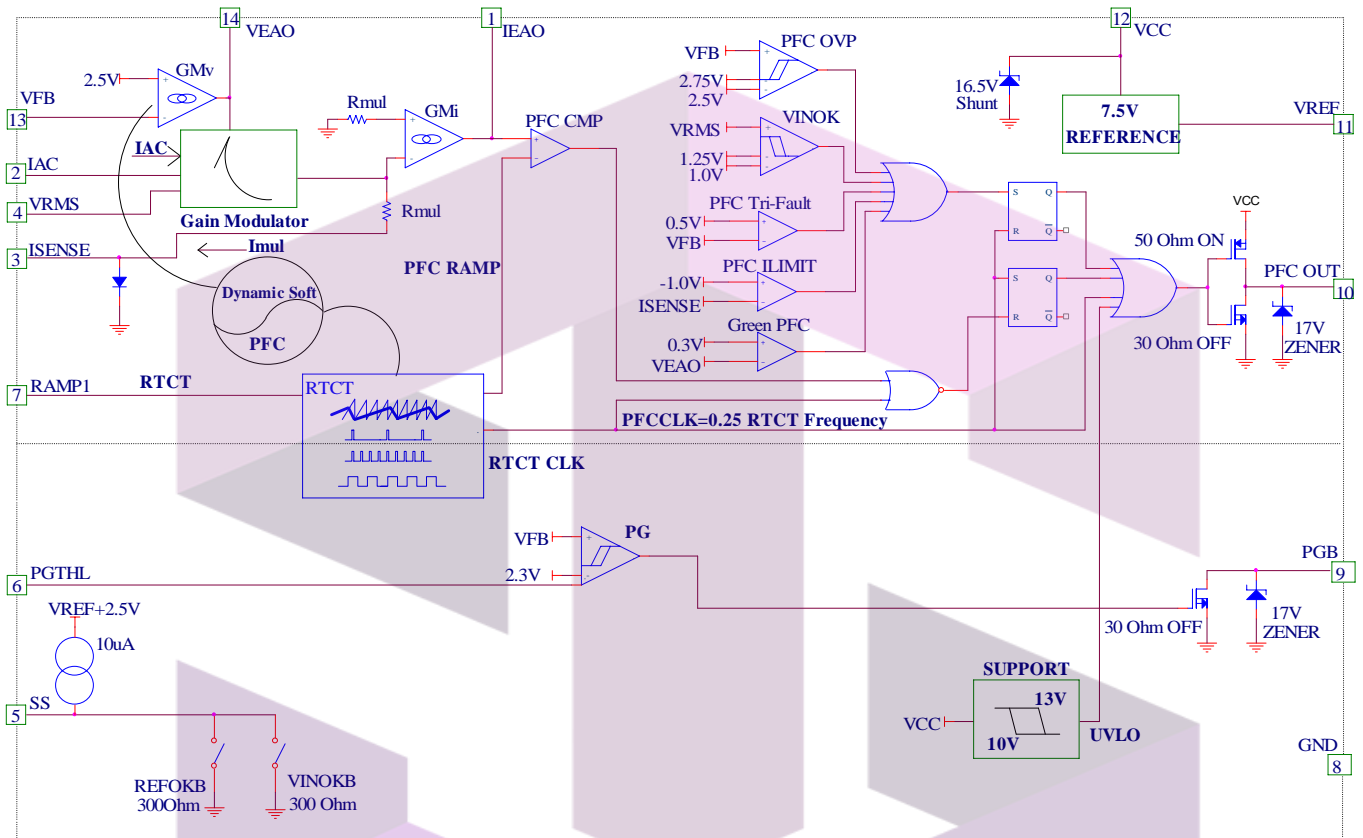


Figure 1. PFC Section Block Diagram

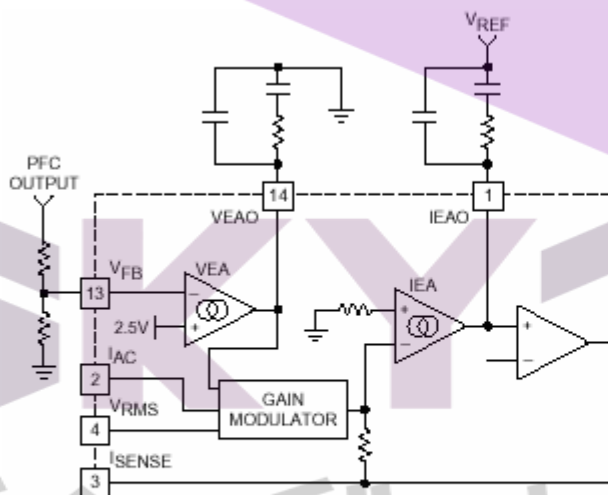


Figure 2. Compensation Network Connections for the Voltage and Current Error Amplifiers

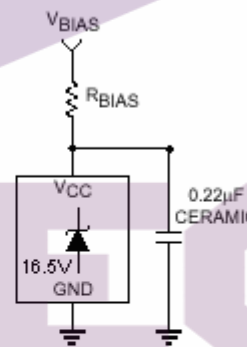


Figure 3. External Component Connections to V_{CC}

Oscillator (RAMP1, or called RTCT)

In CM6502S, $f_{RTCT}=4 \times f_{pwm}=4 \times f_{pfc}$ $f_{RTCT}=200\text{KHz}$, $f_{pwm}=50\text{KHz}$ and $f_{pfc}=50\text{KHz}$ when $V_{EAO}=0\text{V}$, it provides the best performance in the PC application.

The oscillator frequency, f_{RTCT} is the similar formula in CM6800:

$$f_{RTCT} = \frac{1}{t_{RAMP} + t_{DEADTIME}}$$

The dead time of the oscillator is derived from the following equation:

$$t_{RAMP} = C_T \times R_T \times \ln \frac{V_{REF} - 1.25}{V_{REF} - 3.75}$$

at $V_{REF} = 7.5\text{V}$:

$$t_{RAMP} = C_T \times R_T \times 0.51$$

The dead time of the oscillator may be determined using:

$$t_{DEADTIME} = \frac{2.5\text{V}}{4.216\text{mA}} \times C_T = 407.48 \times C_T$$

The dead time is so small ($t_{RAMP} \gg t_{DEADTIME}$) that the operating frequency can typically be approximately by:

$$f_{RTCT} = \frac{1}{t_{RAMP}}$$

C_T should be greater than 470pF.

Let us use 1000PF Solving for R_T yields 7.75K. Selecting standard components values, $C_T = 1000\text{pF}$, and $R_T = 7.75\text{k}\Omega$

The dead time of the oscillator determined two things:

- 1.) PFC minimum off time which is the dead time
- 2.) PWM skipping reference duty cycle: when the PWM duty cycle is less than the dead time, the next cycle will be skipped and it reduces no load consumption in some applications.

Soft Start (SS)

Start-up of the PWM is controlled by the selection of the external capacitor at SS. A current source of $10\mu\text{A}$ supplies the charging current for the capacitor, and start-up of the PWM begins at $SS \sim 1.4\text{V}$. Start-up delay can be programmed by the following equation:

$$C_{SS} = t_{DELAY} \times \frac{10\mu\text{A}}{1.4\text{V}}$$

where C_{SS} is the required soft start capacitance, and the t_{DEADLY} is the desired start-up delay.

It is important that the time constant of the PWM soft-start allow the PFC time to generate sufficient output power for the PWM section. The PWM start-up delay should be at least 5ms.

Solving for the minimum value of C_{SS} :

$$C_{SS} = 5\text{ms} \times \frac{10\mu\text{A}}{1.4\text{V}} = 35\text{nF}$$

Caution should be exercised when using this minimum soft start capacitance value because premature charging of the SS capacitor and activation of the PWM section can result if V_{FB} is in the hysteresis band of the 380V-OK comparator at start-up. The magnitude of V_{FB} at start-up is related both to line voltage and nominal PFC output voltage. Typically, a $0.05\mu\text{F}$ soft start capacitor will allow time for V_{FB} and PFC out to reach their nominal values prior to activation of the PWM section at line voltages between 90Vrms and 265Vrms.

Generating V_{CC}

After turning on CM6502S at 13V, the operating voltage can vary from 10V to 17.9V. That's the two ways to generate V_{CC}. One way is to use auxiliary power supply around 15V, and the other way is to use bootstrap winding to self-bias CM6502S system. The bootstrap winding can be either tapped from PFC boost choke or from the transformer of the DC to DC stage. The ratio of winding transformer for the bootstrap should be set between 18V and 15V.

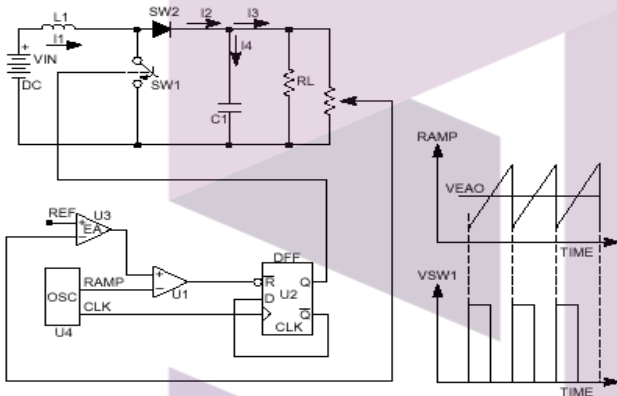


Figure 4. Typical Trailing Edge Control Scheme

In case of leading edge modulation, the switch is turned OFF right at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during OFF time of the switch.

Figure 5 shows a leading edge control scheme. One of the advantages of this control technique is that it required only one system clock. Switch 1(SW1) turns off and switch 2 (SW2) turns on at the same instant to minimize the momentary "no-load" period, thus lowering ripple voltage generated by the switching action. With such synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC's output ripple voltage can be reduced by as much as 30% using this method.

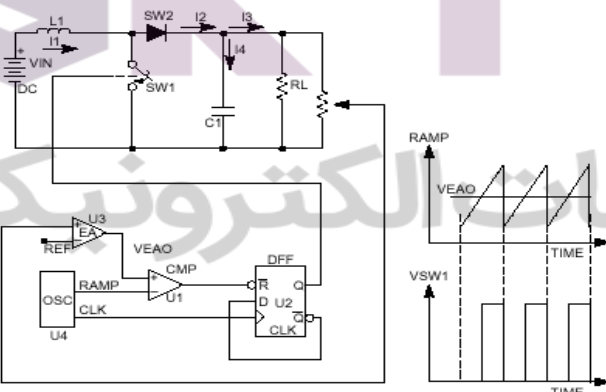


Figure 5. Typical Leading Edge Control Scheme

A filter network is recommended between V_{CC} (pin 13) and bootstrap winding. The resistor of the filter can be set as following.

$$R_{\text{FILTER}} \times I_{\text{VCC}} \sim 2V, I_{\text{VCC}} = I_{\text{OP}} + (Q_{\text{PFCFET}} + Q_{\text{PWMFET}}) \times f_{\text{sw}}$$

$$I_{\text{OP}} = 3\text{mA (typ.)}$$

If anything goes wrong, and V_{CC} goes beyond 19.4V, the PFC gate (pin 12) drive goes low and the PWM gate drive (pin 11) remains function. The resistor's value must be chosen to meet the operating current requirement of the CM6502S itself (5mA, max.) plus the current required by the two gate driver outputs.

EXAMPLE:

With a wanting voltage called, V_{BIAS}, of 18V, a V_{CC} of 15V and the CM6502S driving a total gate charge of 90nC at 100kHz (e.g. 1 IRF840 MOSFET and 2 IRF820 MOSFET), the gate driver current required is:

$$I_{\text{GATEDRIVE}} = 100\text{kHz} \times 90\text{nC} = 9\text{mA}$$

$$R_{\text{BIAS}} = \frac{V_{\text{BIAS}} - V_{\text{CC}}}{I_{\text{CC}} + I_{\text{G}}}$$

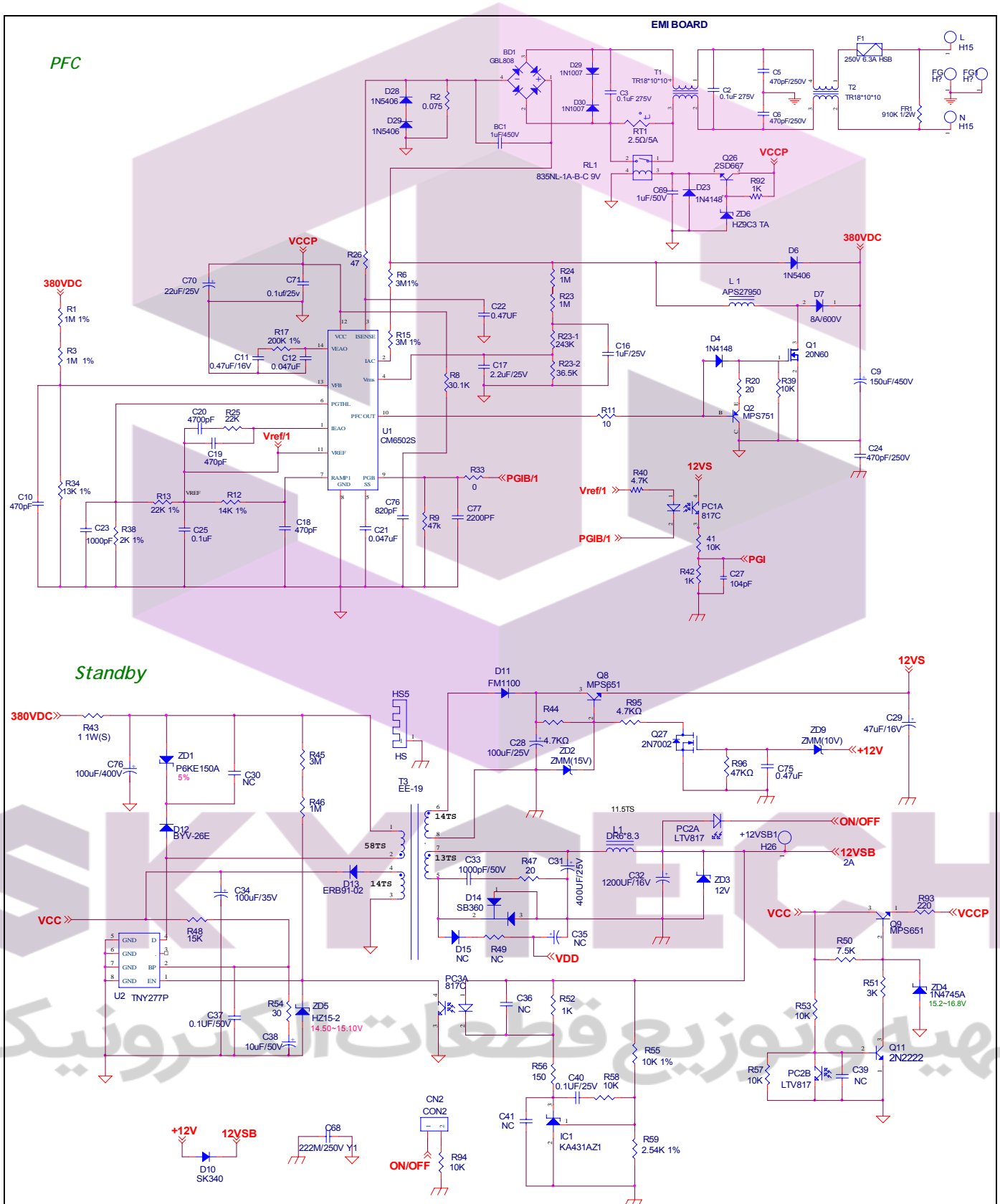
$$R_{\text{BIAS}} = \frac{18\text{V} - 15\text{V}}{5\text{mA} + 9\text{mA}}$$

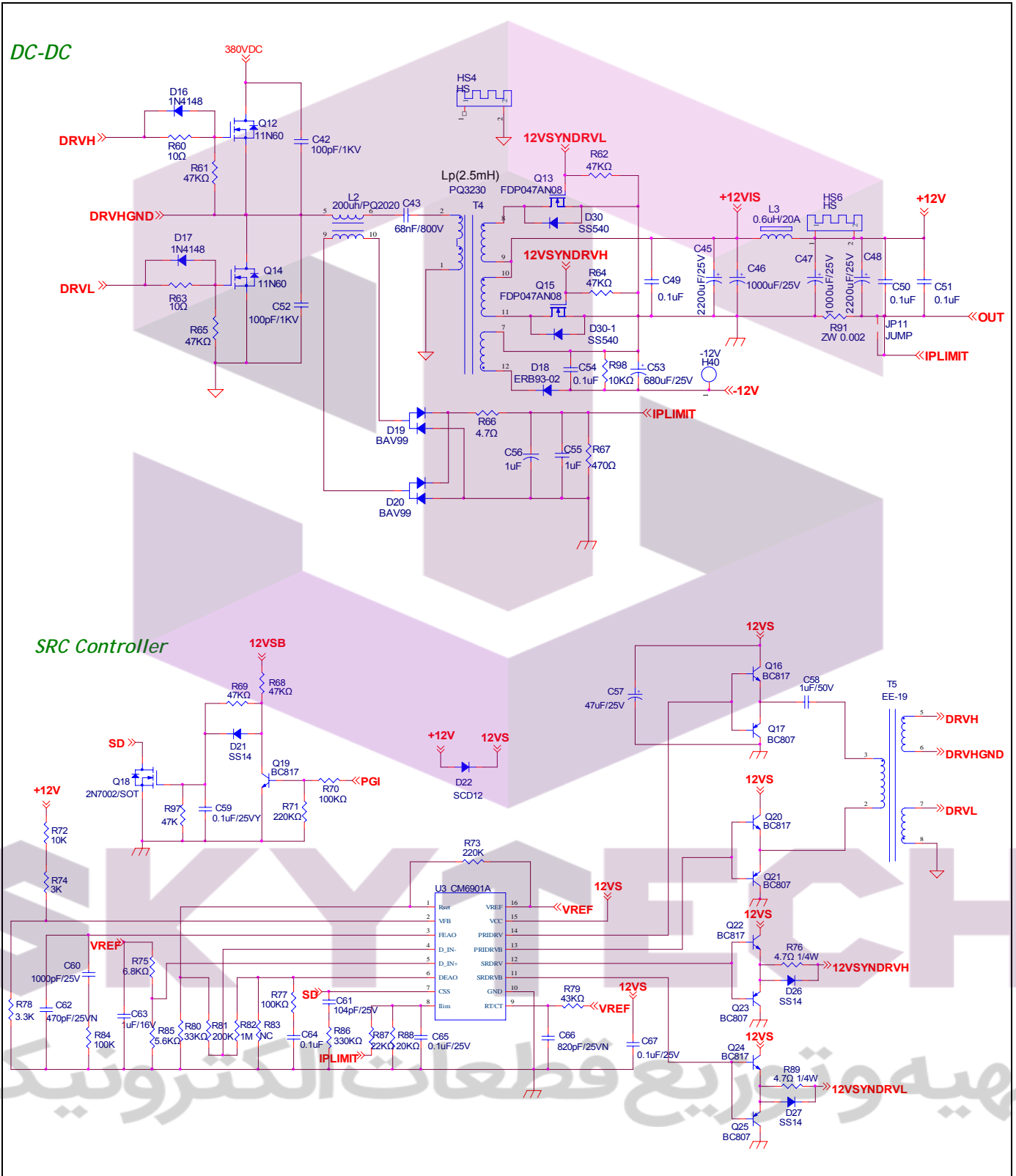
Choose R_{BIAS} = 214Ω

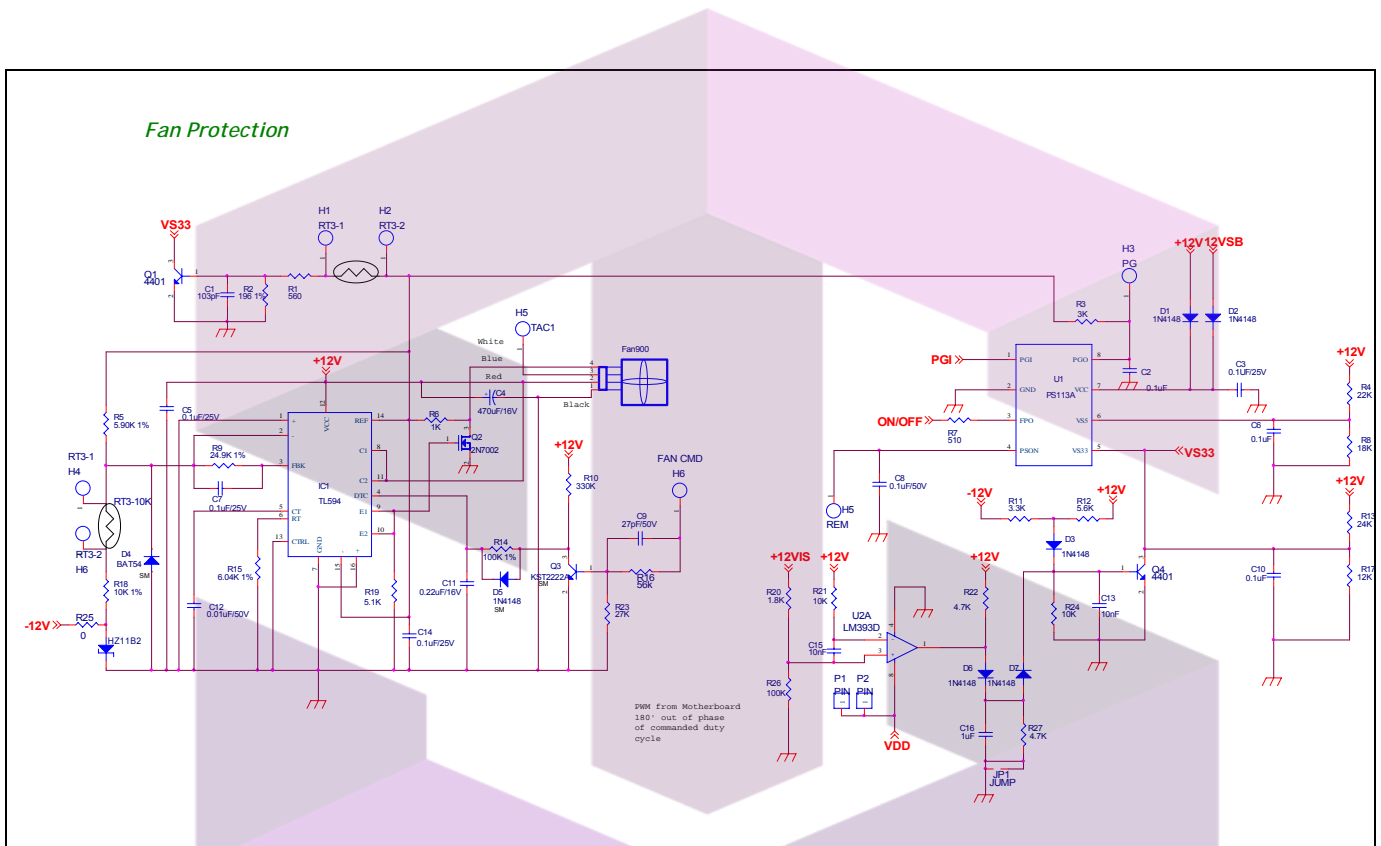
The CM6502S should be locally bypassed with a 1.0μF ceramic capacitor. In most applications, an electrolytic capacitor of between 47μF and 220μF is also required across the part, both for filtering and as part of the start-up bootstrap circuitry.

Leading/Trailing Modulation

Conventional Pulse Width Modulation (PWM) techniques employ trailing edge modulation in which the switch will turn on right after the trailing edge of the system clock. The error amplifier output is then compared with the modulating ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON time of the switch. Figure 4 shows a typical trailing edge control scheme.

APPLICATION CIRCUIT (CM6502S+CM6901A)


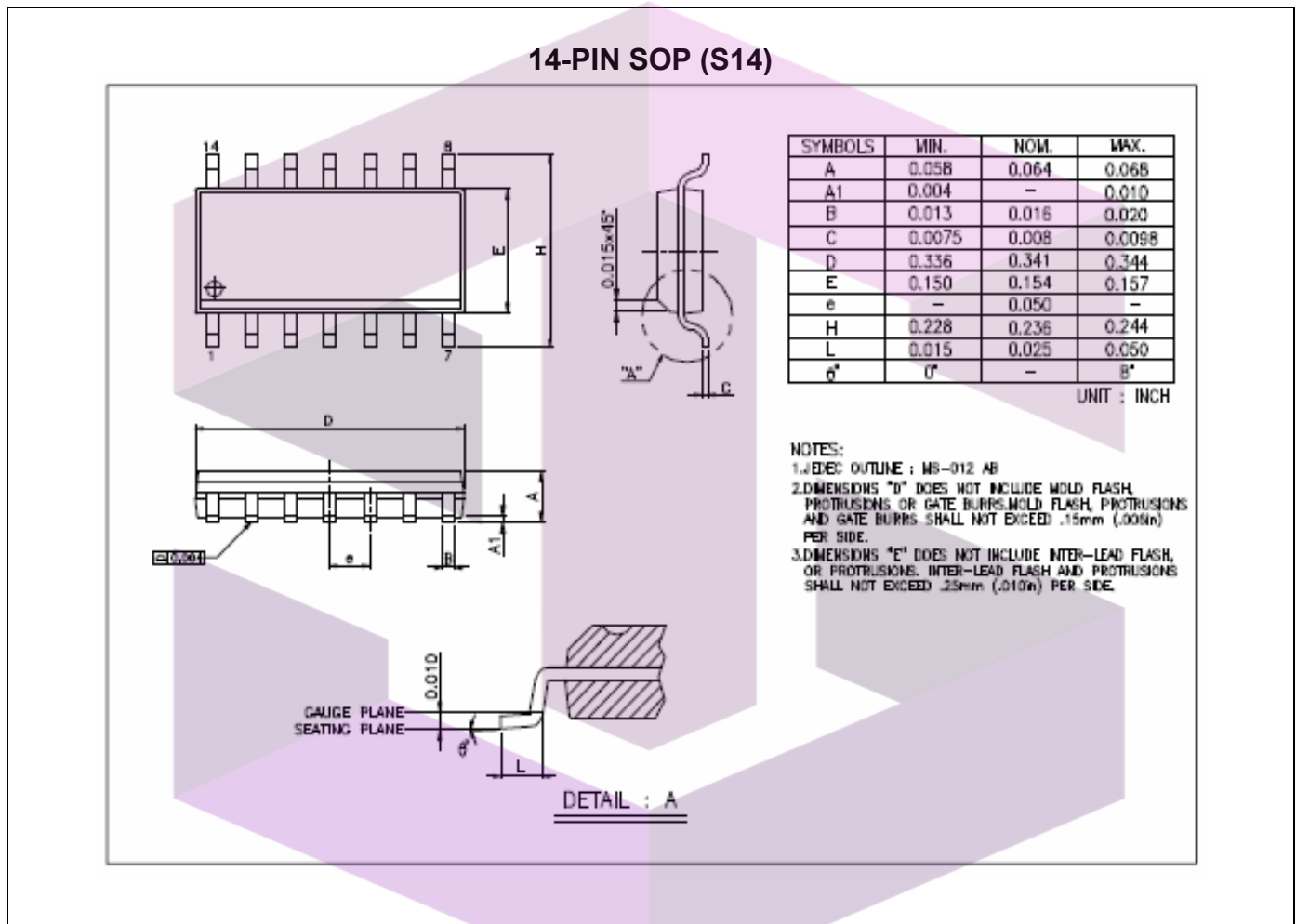




SKYTECH

تهیه و توزیع قطعات الکترونیک

PACKAGE DIMENSION



SKYTECH

تهیه و توزیع قطعات الکترونیک

IMPORTANT NOTICE

Champion Microelectronic Corporation (CMC) reserves the right to make changes to its products or to discontinue any integrated circuit product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

A few applications using integrated circuit products may involve potential risks of death, personal injury, or severe property or environmental damage. CMC integrated circuit products are not designed, intended, authorized, or warranted to be suitable for use in life-support applications, devices or systems or other critical applications. Use of CMC products in such applications is understood to be fully at the risk of the customer. In order to minimize risks associated with the customer's applications, the customer should provide adequate design and operating safeguards.

HsinChu Headquarter

5F, No. 11, Park Avenue II,
Science-Based Industrial Park,
HsinChu City, Taiwan

TEL: +886-3-567 9979

FAX: +886-3-567 9909

<http://www.champion-micro.com>

Sales & Marketing

7F-6, No.32, Sec. 1, Chenggong Rd.,
Nangang District, Taipei City 115
Taiwan, R.O.C.

TEL: +886-2-2788 0558

FAX: +886-2-2788 2985